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Reg. No. :		
Name :	STORE TO COLUMN TO MARIACLE	
	(2008 Scheme	
08.605 : HIGH	I PERFORMANCE MIC	CROPROCESSORS (R)
Time: 3 Hours		Max. Marks: 100
	PART – A	 Disabled pipelining in risc proper
Answer all. Each questi	on carries 4 marks.	What is the Limit cancerof graph
1. Discuss the flag regis	ster of 80486.	S TO STUTITE WE MEMOTY AC
2. Explain the following		DE VIONEMENE COLLIESTITUTE OF 18 AND COLLIESTITUTE OF
PEREQ, PEACK#, RI	EADY#, BUSY#.	Der Sur Sur Sur Sur Sur Sur Sur Sur Sur Su
	of descriptors in segmenta	tion?
4. Explain thread level p	parallelism. SX3 (lilw 1808 to	C Discussifies addressing modes of
5. List the features of R		AO
6. What is delayed bran	ching?	Descripe the 8051 timer
7. What is the advantag 8051?	e and disadvantage of regi	ister indirect addressing mode in
8. Compare and contras	st microprocessors and mi	crocontrollers.
9. What is the role of SE	3F and SCO N registers in	serial data transfer in 8051 ?
10. Discuss IE register in	8051.	(10×4=40 Marks
	PART-B	

Module - 1

11. Describe the architecture of 80386.

10

12. Discuss the different operating modes of 80286.

10

A - 2879 Draw and discuss the paging mechanism of 80386 in detail. 10 14. Explain the on-line cache management of 80486. 10 Module - 2 15. Describe the circular buffer organization of overlapped windows in RISC processors. 10 Discuss pipelining in risc processors. 10 OR 17. What is the significance of graph colouring algorithm in RISC processors? 18. Discuss the different memory addressing modes in ARM processors. Module - 3 19. Write a program to receive the data which has been sent in serial form and sent to Port 0 in parallel form in 8051. 8 20. Discuss the addressing modes of 8051 with examples. 12

10

10

PART - E

OR

22. How the 8051 transfer and receive data serially?

21. Describe the 8051 timer.